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BER Optimization

APPLICATION NOTE

Bit Errror Rate (BER) optimization workflow with Xena's Z800 Freya 112G SerDes Test Modules

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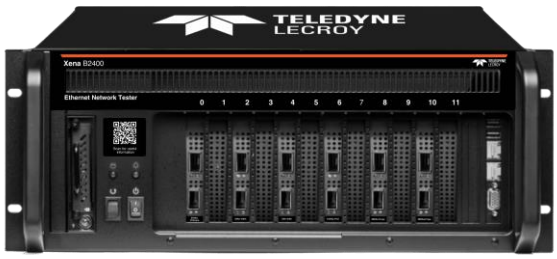
Introduction

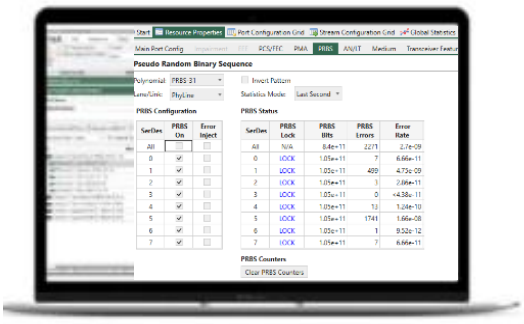
The Link Training (LT) algorithm will get you a good BER, but according to the IEEE standard the LT has to be complete in less than 12 secunds, which is enough to give a good BER. However, if you are looking for the optimal BER, this may take some manual tweaking. Here is an easy way to do that with Z800 Freya and XenaManager.

Due to the way the PAM4 algorithm is designed, it is very common to see a higher BER on some of the uneven lanes, as the example below shows.

Setup

This setup uses two Z800 Freya modules, an 800G electrical cable and XenaManager.





Workflow

1. Open XenaManager and connect to the two Z800 Freya modules
2. Choose the 1 x 800 port config (this config gets you the best results quickly)
3. Click on the 1st port, go to the AN/LT tab under Resource Properties and turn on the "Autoneg and Link Training". Do the same on the opposing port.
4. Go to the PRBS tab and turn on PRBS for all lanes on both ports. Be sure to change the "Statistics Mode" from "Accumulative" to "Last Second"

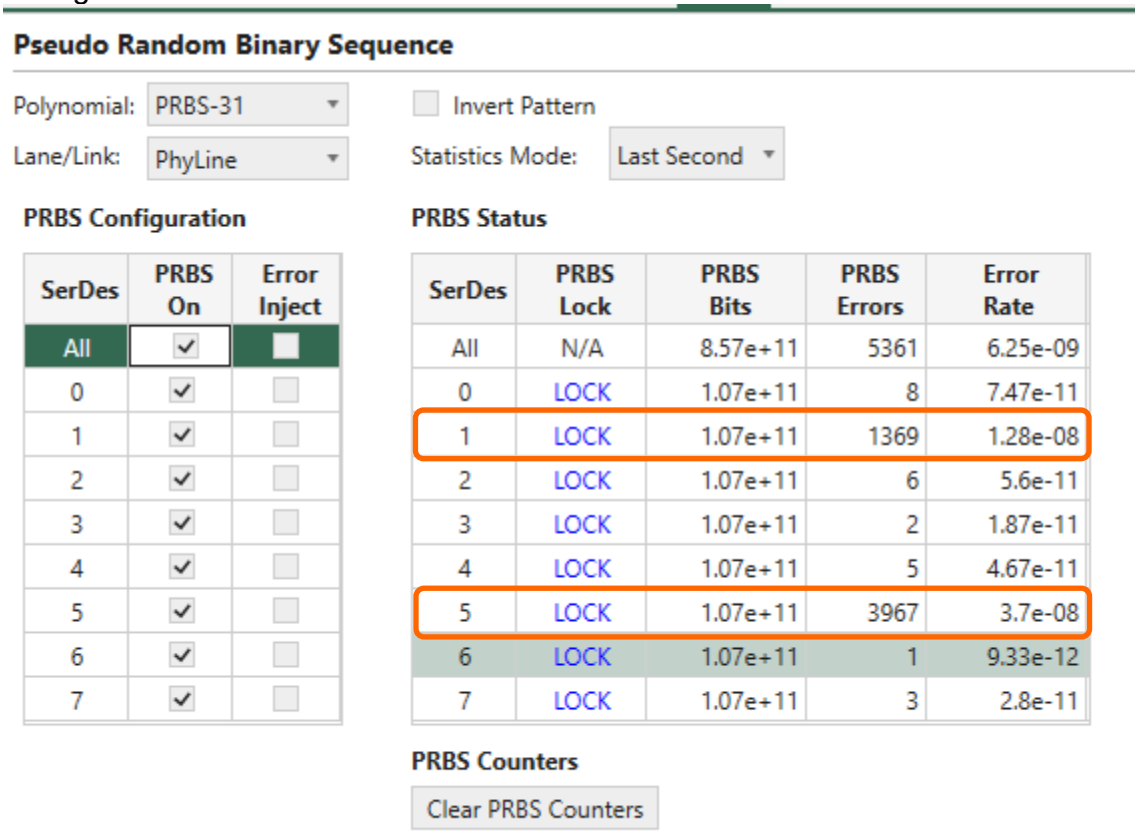


Figure 1: Pseudo Random Binary Sequence overview

5. Now you can make note of the error rate for each of the SerDes. It is a good idea to take a snapshot of this for reference.
6. Find the lanes with the least desirable BER. In this example (Figure 1), it is SerDes #5 with 3.7 e-8, and also SerDes #1.

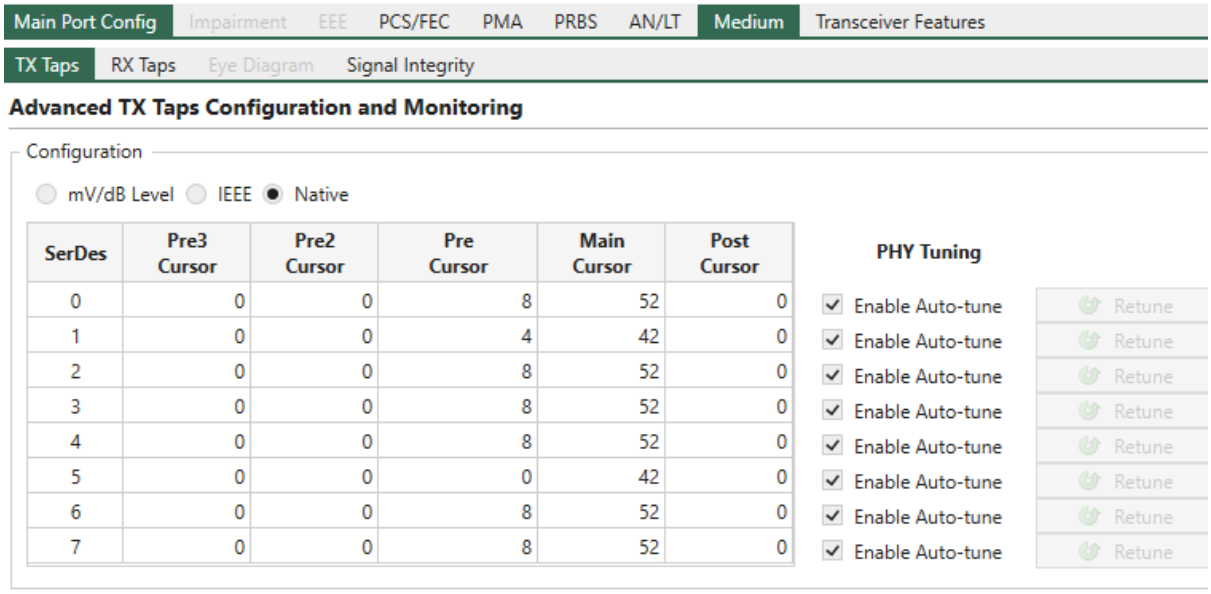


Figure 2: Advances TX Taps Configuration and Monitoring overview

7. Go to the Medium Tab for the opposing port. Note any difference in the settings for lanes #1 and #5 compared to the others. (See Figure 2.)

8. In this case, all the Main cursors are set to 52 except lanes 1 and 5, which are at 42 (using Native figures). And the precursors are different as well. We will now start by bumping the Main from 42 to 47 and see if that improves the BER on the lanes of the opposing port.

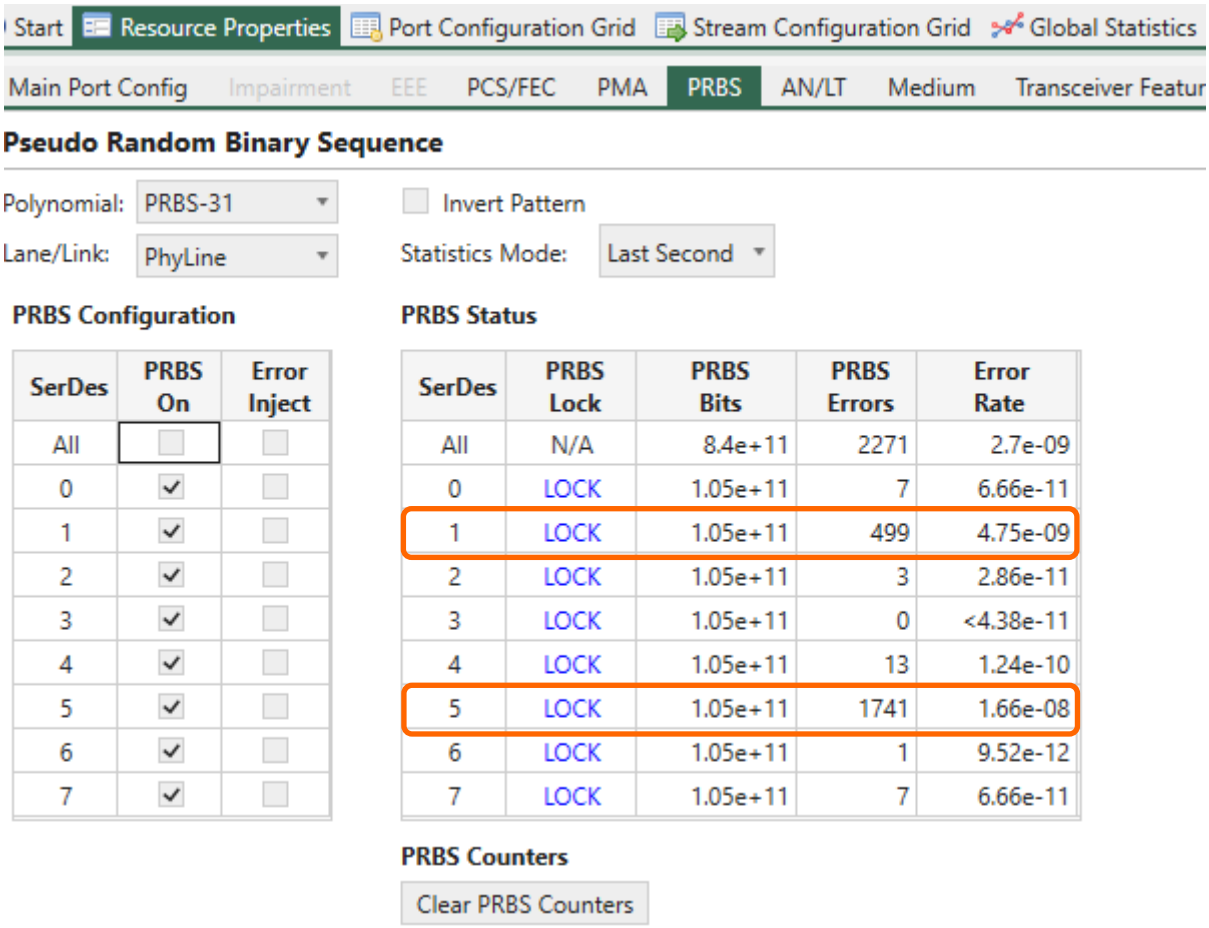


Figure 3: Pseudo Random Binary Sequence overview after initial change

9. In Figure 3, you can see that the BER of lanes 1 & 5 are slightly improved.

10. By play around with the Main tap until it reach a point of negative returns, then do the same with the PreCursor tap.

11. Within ~5 minutes it is possible to settle on settings that significantly improve the overall BER as shown in figure 4.

    In this test example the net overall BER improvement (all lanes) from adjusting the two worst performing lanes went from 6e-9 ==> 2e-10, a significant improvement.

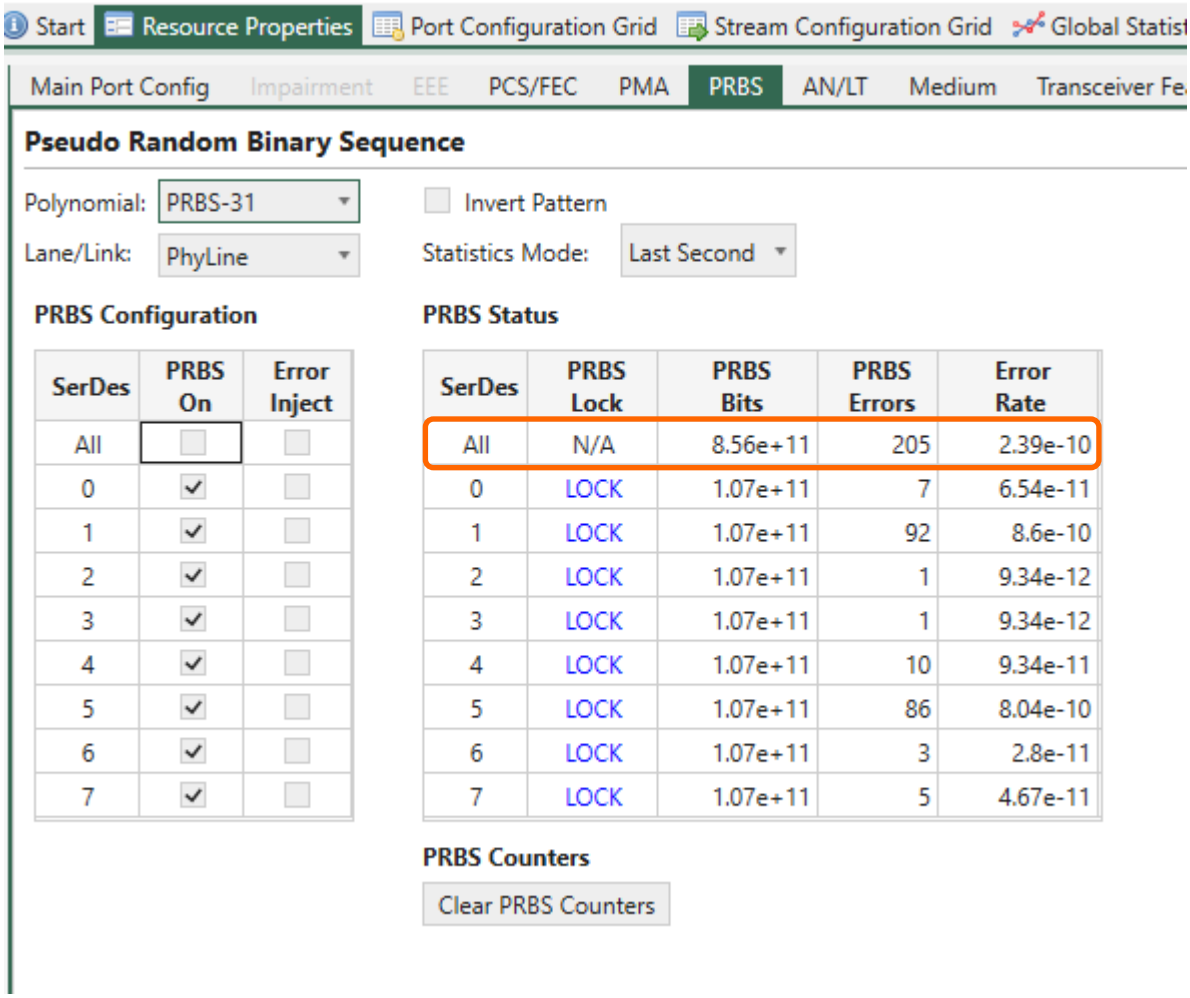


Figure 4: Pseudo Random Binary Sequence overview after further changes

12. Now, if the PRBS is turned off on both ports and the tap settings positions are left in the last adjusted position, check out the PRE-FEC BER in the PCS/FEC tab where it shows the Pre-FEC BER of 2.e-10 matches almost exactly with the final PRBS BER achieved in step 10. *(See figure 5.)*

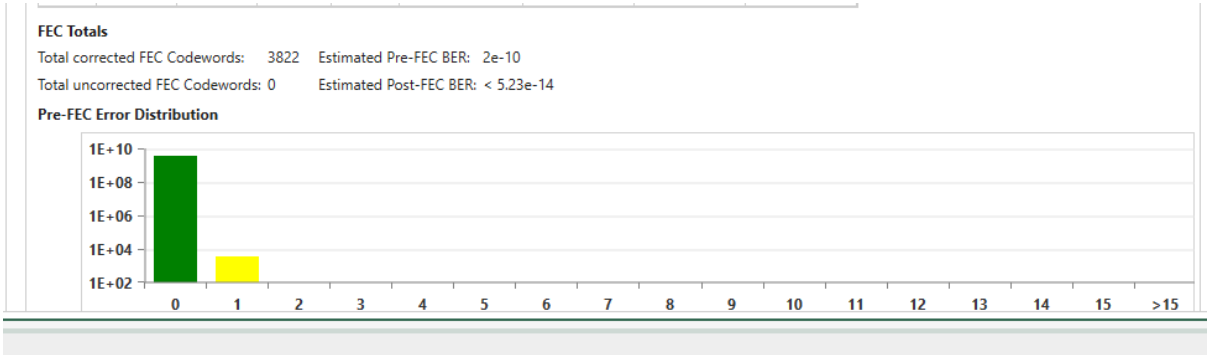


Figure 5: FEC overview

Further tweaking can be performed, but after the Main Cursor, Pre-Cursor, and maybe the Post Cursor are optimized, further improvements are typically minimal.

Learn more about Link Training optimization in this **Technical Note**.