TELEDYNE LECROY
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Verifying SmartNIC ASIC performance at the hardware level using E100 Chimera Network Emulator

CASE STUDY

Background

Smart Network Interface Cards (SmartNICs) are increasingly being deployed in large datacenters to off-load networking services from the Server CPUs. This enables better scalability and security for organizations running large datacenters. In contrast to traditional NICs, SmartNICs offer programmable packet processing, storage, and networking functionality. Furthermore, SmartNICs are designed to monitor key network performance parameters like latency, speed, throughput, and packet loss. SmartNIC interface speeds are typically 100Gbps and above.

A Chinese high-tech startup focused on cloud datacenter ASIC product development is developing network interconnect ASICs for SmartNICs used in large scale datacenters and cloud computing. The company uses Teledyne LeCroy Xena's E100q Chimera network emulator to verify the performance of their new ASIC.

The Challenge

The ability to detect and correct various network impairments is a crucial function of the SmartNIC ASIC. For instance, bit errors are corrected by the Forward Error Correction, short link failures are detected and repaired, out-of-order packets are re-ordered, and latency and jitter are measured. As part of the product development, the Chinese vendor needs to verify the performance of the ASIC when exposed to various network impairments.

It is important that the impairments can be inserted accurately and precisely. For example, to accurately verify the performance of the FEC function, bit errors need to be inserted randomly at the physical layer in a controlled manner. Because the ASIC can detect and repair very short link failures, it is also important to emulate such short link flaps very accurately.

So far, the Chinese vendor has used software-based testers for verification testing. However, these do not have the performance and accuracy required to insert impairments to fully verify the performance of their implementation.

The Solution

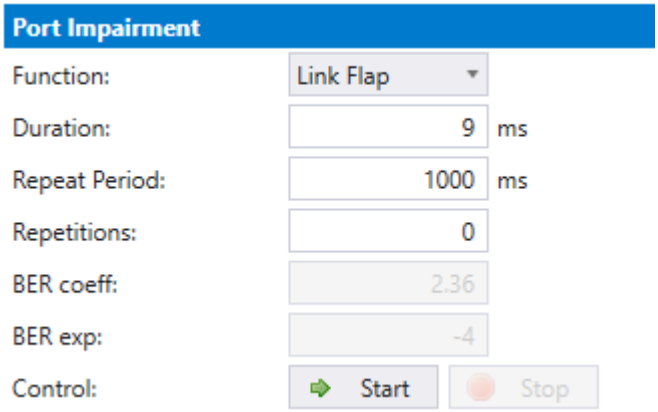
The company decided to try the Teledyne LeCroy Xena E100 Chimera network emulator in their Beijing R&D Center to evaluate if it could deliver the desired accuracy and precision in their product verification.

E100q Chimera can emulate a broad range of network impairments like latency, jitter, packet and port impairments, flexible distributions, and BW shaping. All impairments are supported at five Ethernet speeds: 100GE, 50GE, 40GE, 25GE and 10GE. This flexibility is provided via two physical transceiver cages, both supporting QSFP28 and QSFP+ transceivers. The result is a versatile solution that provides consistent, accurate, well-defined, and repeatable impairments to traffic between network equipment in the lab.

E100q Chimera is ideal for impairment testing of network infrastructure with Ethernet ports capable of supporting up to 100GE. Chimera is easily controlled using the GUI-based XenaManager software.

Using the E100 Chimera's powerful PMA layer error injection function, and its random injection model, the company was able to realistically introduce bit errors to simulate real-world network impairment scenarios.

To verify the ASICs capability to detect a link outage above 10ms, E100 Chimera was used to insert a link flap of precisely 9ms and 11ms, respectively. This test confirmed that the ASIC recovered from the 11ms link outage as expected.



Another important function of the SmartNIC ASIC is to correct out-of-order packet sequences arising from, for instance, load balancing. With E100 Chimera, it was possible to arrange a deliberate wrong ordering of packets as shown on Figure 1. By transmitting this packet sequence through the SmartNIC ASIC it was verified that the product corrected the out-of-order sequence as shown on Figure 2.

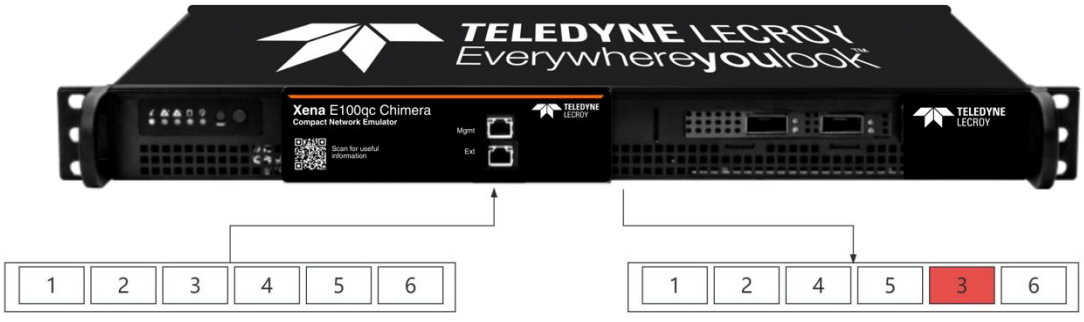


Figure 1: Deliberate wrong ordering pf flow with E100q Chimera.

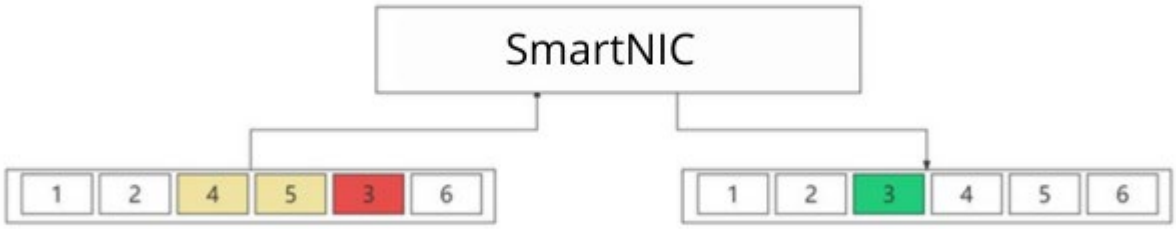


Figure 2: The SmartNIC corrects the out-of-order data.

The E100 Chimera impairment tester also allowed the delay and jitter of various distribution models to be emulated with high accuracy. Delay impairments from the microsecond to the second level at wire speed were inserted. In this way, it was possible to accurately test the perception of different delays of ASICS and smart network cards.

SUMMARY

SmartNICs are replacing traditional NICs in large datacenters to improve scalability and security. By incorporating programmable packet processing, storage, and networking functionality, SmartNICs can off-load networking services from the server CPU. Furthermore, SmartNICs are designed to monitor and recover from key network impairments.

A Chinese vendor developing ASICs for SmartNICs needed an accurate and precise, hardware-based test solution to verify their product design. Previously, they had used a software-based tester but that was not accurate enough.

The E100 Chimera was a very cost-effective network emulation solution that made it easy for them to fully verify the performance of their product and thereby offer a better product for their customers.