CHIMERA

RELEASE 4

5-speed 2-port network impairment emulator

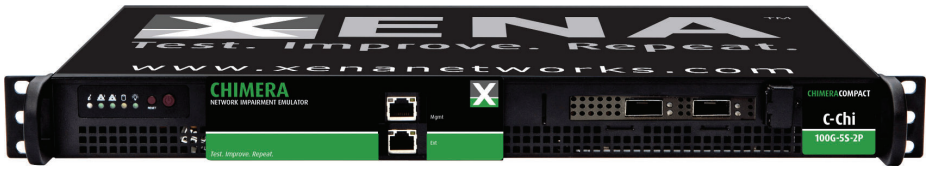
Chimera can emulate network impairment at five Ethernet speeds: 100GE, 50GE, 40GE, 25GE and 10GE. This unique flexibility is provided via two physical transceiver cages, both supporting QSFP28 and QSFP+ transceivers.

The result is a versatile solution that provides consistent, accurate, well-defined and repeatable impairments to traffic between DUTs in the lab. Chimera is ideal for benchmarking, stress/negative, "what-if" and regression testing of network infrastructure and Ethernet equipment capable of supporting 100GE such as switches, routers, NICs and fronthaul/ backhaul platforms.

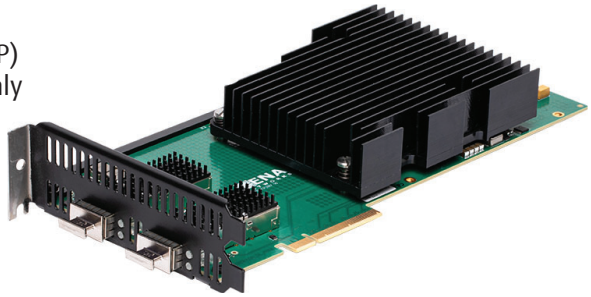
Chimera is easily controlled using ValkyrieCLI scripting, making automation of tests simple using the Python library supplied by Xena.

TOP FEATURES

- Industry's only fully integrated traffic generation & impairment solution (Valkyrie & Chimera)
- Multi-speed impairment – 10/25/40/50 & 100GE – in a compact 1U chassis or as a ValkyrieBay test module
- High port density
- Flexible port reservation
- Ease of use
- Free software (incl. ValkyrieManager and ValkyrieCLI scripting)
- Free tech support & training for product lifetime



Chimera is available as standalone ChimeraCompact (P/N: C-Chi-100G-5S-2P) and as a 2-slot test module (P/N: C-Chi-100G-5S-2P) for the ValkyrieBay (only Val-C12-2400G)



SYSTEM OVERVIEW

Interface category	QSFP28 • 100G, 50G, 40G*, 25GE and 10G* Ethernet QSFP+ • 40G, 10G Ethernet * *Depending on transceiver capabilities*
Total number of test ports (software configurable)	2x100G, 4x50G, 2x40G, 8x25G and 8x10G Ethernet
Interface options	Each cage • 1 x 100GBASE-SR4/LR4/CR4, or 802.3bj standard • 2 x 50GBASE-SR2/LR2/CR2, or Consortium** • 1 x 40GBASE-SR4/LR4/CR4, or 802.3ba • 4 x 25GBASE-SR/LR/CR, or 802.3by/Consortium** • 4 x 10GBASE-SR/LR/CR 802.3ae Actual interface options depend on the capabilities of the inserted transceiver. Both cages must run with the same base interface configuration (e.g. 2 x 50G). ** *As defined by 25/50 Gigabit Ethernet Consortium*
Forward Error Correction (FEC)	• RS-FEC (Reed Solomon) FEC, IEEE 802.3 Clause 91 (100GE) • RS-FEC (Reed Solomon) FEC, IEEE 802.3 Clause 108 (25GE) • RS-FEC (Reed Solomon) FEC, 25G Ethernet Consortium (25GE)
Number of transceiver module cages	2 x QSFP28/QSFP+
Port statistics	Link state, FCS errors, frame and byte counters
SyncE	Lock Tx clock to recovered Rx clock from any input port (Single clock domain)
Field upgradeable	System is fully field upgradeable to product releases (FPGA images and software)
Tx disable	Enable/disable of optical laser
Oscillator characteristics	• Initial Accuracy is 3 ppm • Frequency drift over 1st year: +/- 3 ppm (over 15 years: +/- 15 ppm) • Temperature Stability: +/- 20 ppm (Total Stability is +/- 35 ppm)

NOTE: Features in green will be made available in future releases.

RELEASE 4

100/50/40/25GE FRAMED PRBS AND PCS LAYERS

Link Flap	Single short or repeatable link down events with ms precision
Error Injection (PMA Layer)	Single short or repeatable error inject periods at PMA layer with ms precision
Supported frame sizes	Ethernet packets from 56 to 12288 bytes

FLOWS

Number of flows per port	8 (incl. default flow)
Flow filter definition	• MAC Source and Destination Address • VLAN Tag (C-Tag and S-Tag) • MPLS Label • IPv4 Source and Destination Address • IPv4 DSCP/TOS • IPv6 Source and Destination Address • UDP/TCP port numbers • Up to 6 consecutive bytes in the packet • Xena Test Payload ID (TID)
Flow statistics	Chimera implements impairment counters per flow, including dropped, corrupted, mis-ordered and duplicated packets.
Libraries	Libraries of own impairments

IMPAIRMENT PER FLOW

General	Impairments can be changed dynamically
Packet Manipulation	Packet drop Duplication Mis-ordering Protocol Corruption (Ethernet Frame FCS, IP/UDP/TCP header Check Sum error) • Custom Payload Corruption (with correct Ethernet FCS)
Latency / Jitter	Constant latency • Max. latency lossless 160ms (100GE wire-speed) Step-size 100 ns, accuracy: +/- 50 ns • Max. latency reduced bandwidth 1.6 s (19.5 sec) • Min. (Intrinsic) delay: 7.0 µs for 10G/40G/50G/100G 7.2 us for 25G 13.0 us for 10G Accumulate & Burst Step (2 alternating delays) Jitter (Distributions - see below)
Flexible Distributions	Drop, duplication and corruption probability is configurable up to 100%. Step size: 0.0001% Impairments and jitter (Duplication, Drop, Corruption and latency) can be applied with very flexible distributions including Random, Periodic, Gilbert-Elliot, Gaussian, Gamma and Uniform. You can also specify custom distributions to be used with impairments.
Bandwidth Control (L1 / L2)	Policing - Step size: 100 kbps Shaping - Step size: 100 kbps

HARDWARE SPECIFICATIONS

Dimensions (installed in a 1U ChimeraCompact)	• W: 19" (48.26 cm) / H: 1.75" (4.45 cm) / D: 9.8" (25 cm) • Weight: 10 lbs (4.5 kg)
Power	• AC Voltage: 100-240V • Frequency: 50-60Hz • Max. Power: 90W (ValkyrieCompact) / 120W (ValkyrieBay) • Max. Current: 0.8A with 120V supply, and 0.4A with 240V supply
Max. Noise	• ChimeraCompact: 49 dBa • ValkyrieBay: 58.5 dBa
Environmental	• Operating Temperature: 10 to 35° C • Storage Temperature: -40 to 70° C • Humidity: 8% to 90% non-condensing
Regulatory	• FCC (US), CE (Europe)

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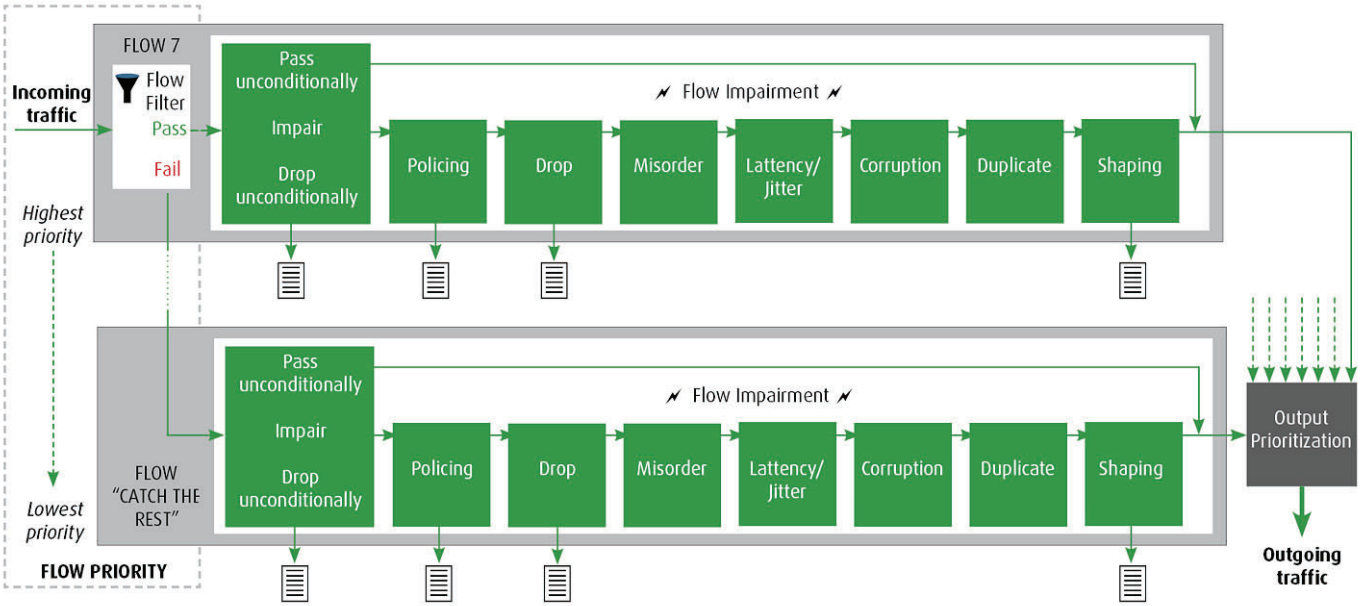
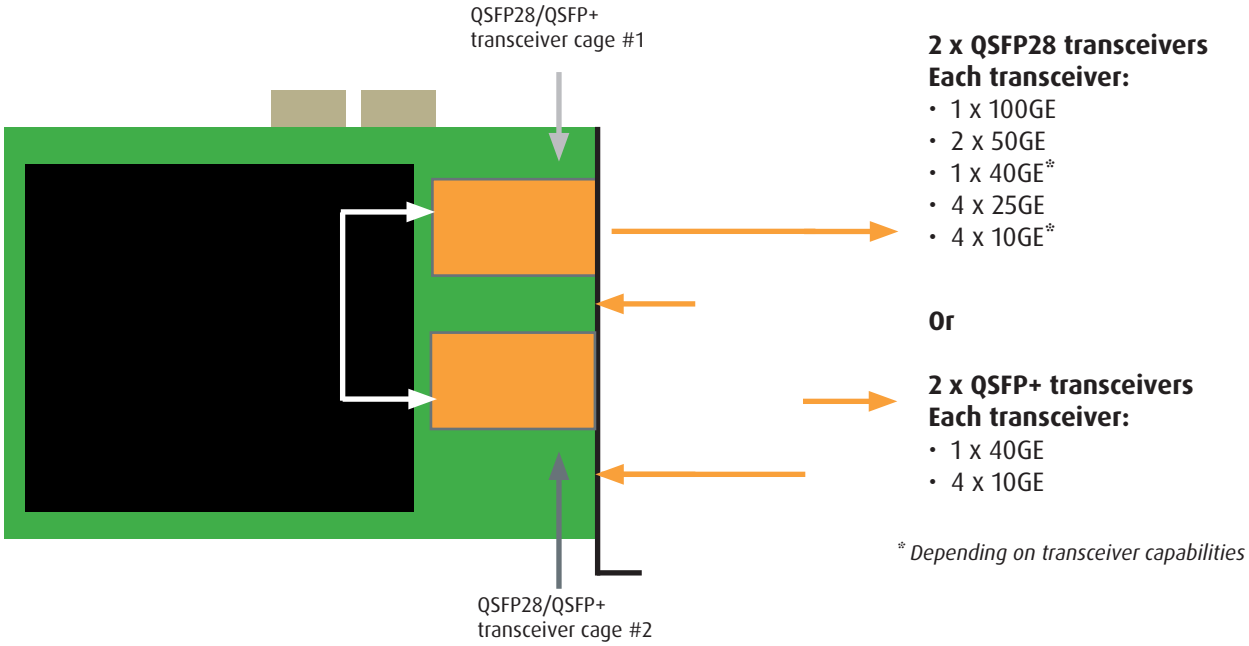
How Chimera processes incoming traffic:



One module - multiple options

Chimera has 2 transceiver cages. The type of transceiver used determines the speeds and number of ports available. The port number / speed configuration must be the same for both cages and this is defined using ValkyrieManager, Xena's traffic generation and analysis software.



2 x QSFP28 transceivers
Each transceiver:
- 1 x 100GE
- 2 x 50GE
- 1 x 40GE*
- 4 x 25GE
- 4 x 10GE*

Or

2 x QSFP+ transceivers
Each transceiver:
- 1 x 40GE
- 4 x 10GE

* *Depending on transceiver capabilities*

PRODUCT NUMBERS (P/N)

- Chi-100G-5S-2P - test module for ValkyrieBay chassis
- C-Chi-100G-5S-2P- mounted in ValkyrieCompact chassis

XENA™
Test. Improve. Repeat.