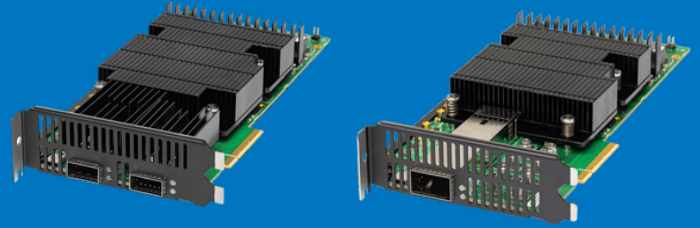


# Z800 Freya

## 5-speed 800Gbps (112/56G SerDes) QSFP and OSFP Test modules



### Key Features

- 5-speeds: 800GE, 400GE, 200GE, 100GE & 50GE
- Dual media: QSFP-DD800 & QSFP112 or OSFP
- Supports 112G SerDes (PAM4 112G) & 56G SerDes (PAM4)
- Xena PHY for unique Layer 1 insight
- Test with or of optics, AECs, ACCs and DAC's
- Auto-Negotiation & Link Training (AN/LT)
- Advanced Physical Layer testing
- Price/performance
- Ease of use

[Find out more here:](#)



**Z800 Freya traffic generators are available with QSFP or OSFP interfaces and support five different Ethernet network speeds - 800GE, 400GE, 200GE, 100GE and 50GE using 112G/56G SerDes (PAM4 112G/56G).**

Z800 Freya is a highly versatile solution designed for performance and functional testing of Ethernet network infrastructure and equipment including switches, routers and NICs.

Z800 Freya is unique on the market with its ability to test up to 800GE with 112G SerDes (PAM4 112G) meeting the highest demands for superior signal integrity and Bit Error Rate (BER) performance.

Z800 Freya supports extensive L1 test features, and the integrated Xena PHY provides unique insights to advanced PCS and PMA layer testing including dynamic transceiver clock sweep, lane skewing and PRBS modes. Signals can be analyzed in advanced Signal Integrity View (SIV), to provide visual information on signal quality.

Z800 Freya traffic generators support Auto-Negotiation and Link Training (AN/LT) on 112G SerDes and 56G SerDes.

Z800 Freya modules can be installed in Xena B2400 chassis for multi-module setup, or delivered in the XenaCompact chassis, making it the smallest and lightest 800G Ethernet test solution in the market.

It comes complete with XenaManager, the intuitive multi-user management software for generating and analyzing traffic. Also included is Xena OpenAutomation (XOA), an open-source scripting and automation framework designed to help test engineers make the most of Xena testers with tailored tests and standardized test methodologies.

### Ethernet Auto-Negotiation & Link Training Test Tools

Z800 Freya customers can purchase a Z800 Freya-ANLT license for enabling the AN/LT Utility on Z800q Freya and Z800o Freya OSFP modules. This license makes additional AN/LT tools available for thorough testing of the endpoint behaviour during AN and LT process.

The AN/LT Utility provides insight, visibility, and configuration possibilities to the AN and LT process making it easy to analyze DUT behaviour during AN/LT, configure and optimize the relevant AN parameters and LT coefficients.

PORT LEVEL FEATURES																																																				
Interface category	<p><b>Z800q Freya:</b></p> <ul style="list-style-type: none"> <li>• <b>QSFP-DD800</b> 800G, 400G, 200G, 100G, 50G Ethernet</li> <li>• <b>QSFP112</b> 400G, 200G, 100G, 50G Ethernet</li> </ul> <p><b>Z800o Freya:</b></p> <ul style="list-style-type: none"> <li>• <b>OSFP</b> 800G, 400G, 200G, 100G, 50G Ethernet</li> </ul>																																																			
Total number of test ports (software configurable)	1x800G, 2x400G, 4x200G, 8x100G or 8x50G Ethernet																																																			
Interface options	<p>QSFP-DD800 &amp; OSFP cage</p> <table> <tr> <td>112G SerDes:</td> <td>Line code:</td> <td>IEEE:</td> </tr> <tr> <td>1 x 800GE</td> <td>PAM4</td> <td>802.3df (D2.0) / ETC* or</td> </tr> <tr> <td>2 or 1 x 400GE</td> <td>PAM4</td> <td>802.3ck or</td> </tr> <tr> <td>4 or 2 x 200GE</td> <td>PAM4</td> <td>802.3ck or</td> </tr> <tr> <td>8 or 4 x 100GE</td> <td>PAM4</td> <td>802.3ck</td> </tr> </table> <p>56G Serdes:</p> <table> <tr> <td>1 x 400GE</td> <td>PAM4</td> <td>802.3bs or 802.3cd</td> </tr> <tr> <td>2 x 200GE</td> <td>PAM4</td> <td>802.3cd or</td> </tr> <tr> <td>4 x 100GE</td> <td>PAM4</td> <td>802.3cd or</td> </tr> <tr> <td>8 x 50GE</td> <td>PAM4</td> <td>802.3cd</td> </tr> </table> <p>QSFP112 cage</p> <table> <tr> <td>112G SerDes:</td> <td>Line code:</td> <td>IEEE:</td> </tr> <tr> <td>1 x 400GE</td> <td>PAM4</td> <td>802.3ck or</td> </tr> <tr> <td>2 x 200GE</td> <td>PAM4</td> <td>802.3ck or</td> </tr> <tr> <td>4 x 100GE.</td> <td>PAM4</td> <td>802.3ck</td> </tr> </table> <p>56G Serdes:</p> <table> <tr> <td>1 x 400GE</td> <td>PAM4</td> <td>802.3bs or 802.3cd</td> </tr> <tr> <td>2 x 200GE</td> <td>PAM4</td> <td>802.3cd or</td> </tr> <tr> <td>4 x 100GE</td> <td>PAM4</td> <td>802.3cd or</td> </tr> <tr> <td>8 x 50GE</td> <td>PAM4</td> <td>802.3cd</td> </tr> </table> <p>Both cages must run with the same interface configuration (e.g. 4 x 100G) and same SerDes speed (e.g 112G)</p> <p>*ETC = Ethernet Technology Consortium</p>	112G SerDes:	Line code:	IEEE:	1 x 800GE	PAM4	802.3df (D2.0) / ETC* or	2 or 1 x 400GE	PAM4	802.3ck or	4 or 2 x 200GE	PAM4	802.3ck or	8 or 4 x 100GE	PAM4	802.3ck	1 x 400GE	PAM4	802.3bs or 802.3cd	2 x 200GE	PAM4	802.3cd or	4 x 100GE	PAM4	802.3cd or	8 x 50GE	PAM4	802.3cd	112G SerDes:	Line code:	IEEE:	1 x 400GE	PAM4	802.3ck or	2 x 200GE	PAM4	802.3ck or	4 x 100GE.	PAM4	802.3ck	1 x 400GE	PAM4	802.3bs or 802.3cd	2 x 200GE	PAM4	802.3cd or	4 x 100GE	PAM4	802.3cd or	8 x 50GE	PAM4	802.3cd
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Auto Negotiation and Link Training	<p>Auto-negotiation: IEEE 802.3 Clause 73 and ETH. 400G/800G specifications</p> <p>Link training: IEEE 802.3 Clause 136 and 161</p>																																																			
Forward Error Correction (FEC)	<p>RS-FEC (Reed-Solomon) (544,514,t=15), IEEE802.3 Clause 119</p> <p>RS-FEC (Reed-Solomon) (544,514,t=15), IEEE802.3 Clause 134</p> <p>RS-FEC (Reed-Solomon) (544,514,t=15), IEEE802.3 Clause 161 for 100GBASE</p>																																																			
Number of transceiver module cages	<p>Z800q: 1 x QSFP-DD800 and 1 x QSFP112</p> <p>Z800o: 1 x OSFP</p>																																																			
Port statistics	<p>Link state, FCS errors, pauseframes, ARP/PING, error injections, training packet</p> <p>All traffic: RX and TX Mbit/s, packets/s, packets, bytes</p> <p>Traffic w/o test payload: RX and TX Mbit/s, packets/s, packets, bytes</p>																																																			
Adjustable Inter FrameGap (IFG)	Configurable from 16 to 56 bytes, defaultis 20B (12BIFG + 8B preamble)																																																			

PORT LEVEL FEATURES	
Transmit line rate adjustment	Ability to adjust the effective line rate by forcing idle gaps equivalent to -1000 ppm (increments of 10 ppm)
Transmit line clock adjustment	From -400 to 400 ppm in steps of 1 ppm (shared across all ports)
PPM Sweep	Configurable linear or step sweep +/- 400 ppm
ARP/PING	Supported (configurable IP and MAC address per port)
Field upgradeable	System is fully field upgradeable to product releases (FPGA images and software)
Tx disable	Enable/disable of optical laser or copperlink
Field upgradeable	System is fully field upgradeable to product releases (FPGA images and software)
IGMPv2 multicast join/leave	IGMPv2 continuous multicast join, with configurable repeat interval
Histogram statistics	Two real-time histograms per port. Each histogram can measure one of RX/TX packet length, IFG, or Latency distribution for all traffic, a specific stream, or a filter
Loopback modes	<ul style="list-style-type: none"> <li>• L1RX2TX – RX-to-TX, transmit byte-by-byte copy of the incoming packet</li> <li>• TXON2RX – TX-to-RX, packet is also transmitted from the port</li> <li>• TXOFF2RX – TX-to-RX, port's transmitter is idle</li> </ul>
Oscillator characteristics	<ul style="list-style-type: none"> <li>• Initial Accuracy is 3 ppm</li> <li>• Frequency drift over 1st year: +/- 3 ppm (over 15 years: +/- 15 ppm)</li> <li>• Temperature Stability: +/- 20 ppm (Total Stability is +/- 35 ppm)</li> </ul>
I2C RX/TX transceiver access speed	To a maximum of 800KHz (actual speed depends on medium support)
Electrical cables	<p>Both Passive and Active electrical cables are supported:</p> <ul style="list-style-type: none"> <li>• DACs tested up to 2,5-meter cable*</li> <li>• ACCs tested up to 4-meter cable*</li> <li>• AECs tested up to 7-meter cable*</li> </ul> <p>*Length might vary dependent on vendor</p>

PCS/PMA LAYERS TESTING	
Payload Test pattern	PRBS-13Q, PRBS-31Q, SSPRQ test pattern (IEEE 802.3 Clause 120.5.11.2.3) and Square Wave (IEEE 802.3 Clause 120.5.11.2.4).
Alarms	PRBS pattern loss, link sync loss
Error analysis	Bit-errors: seconds, count, rate
PCS virtual lane configuration	User-defined skew insertion per Tx virtual lane, and user-defined virtual lane-to-SerDes mapping for testing of the Rx PCS virtual lane reorder function
PCS virtual lane statistics	Relative virtual lane skew measurements (up to 2048 bits) Corrected Bit error, Pre-FEC BER
FEC Total statistics	Total corrected FEC symbols, Total uncorrected FEC symbols, Estimated Pre-FEC BER, Estimated Post-FEC BER, Pre-FEC Error Distribution Graph
Link Flap	Single shot or repeatable link-down events with ms precision
Error Injection (PMA Layer)	Repeatable error inject periods at PMA layer with ms precision

PHY/TRANSCEIVER ETHERNET TESTING	
Programmable Pattern Generator	Supported in Layer 1/ANLT mode: <ul style="list-style-type: none"> <li>• Single stream Ethernet frames with FCS</li> <li>• Traffic load: up to 100%</li> <li>• Configurable Frame Size distribution and content</li> <li>• Transmit and Receive Statistics</li> <li>• No latency and jitter measurement, No Filter and No capture supported</li> </ul>

ADVANCED PHY FEATURES	
Equalization Controls	Tx Transmit Equalization Controls <ul style="list-style-type: none"> <li>• Pre-emphasis</li> <li>• Attenuation</li> <li>• Post-emphasis</li> </ul> Rx Receive Equalization Controls <ul style="list-style-type: none"> <li>• Continuous Time Linear Equalizer</li> </ul>
Signal Integrity Analysis	Advanced Signal Integrity View for PAM4 modulated signal quality analysis

TRANSMIT ENGINES	
Number of transmit streams per port	256 (wire-speed) Each stream can generate millions of traffic flows using field modifier
Test payload insertion per stream	Wire-speed packet generation with timestamps, sequence numbers, and data integrity signature optionally inserted into each packet.
Stream statistics	TX Mbit/s, packets/s, packets, bytes, FCS error
Bandwidth profiles	Burst size and density can be specified. Uniform and bursty bandwidth profile streams can be interleaved
Field modifiers	24-bit header field modifiers with incremental, decremental, or random mode. Each modifier has configurable bit-mask, repetition, min, max, and step parameters. Eight 24-bit modifiers can be configured per stream
Packet length controls	Fixed, random, butterfly, and incrementing packet length distributions from 56 to 16k bytes
Packet payloads (basic)	Repeated userspecified 1 to 18B pattern, an 8-bit incrementing pattern
Error generation	Undersize length (56 bytes min) and oversize length (12288 bytes max.) packet lengths, injection of sequence, disorder, payload integrity, and FCS errors
TX packet header support and RX auto decodes	Ethernet, Ethernet II, VLAN, ARP, IPv4, IPv6, UDP, TCP, LLC, SNAP, GTP, ICMP, RTP, RTCP, STP, MPLS, PBB, or fully specified by user
Packet scheduling modes	<ul style="list-style-type: none"> <li>• Normal (stream interleaved mode) – standard scheduling mode, precise rates, minor variation in packet inter-frame gap.</li> <li>• Strict Uniform – new scheduling mode, with 100% uniform packet inter-frame gap, minor deviation from configured rates.</li> <li>• Sequential packet scheduling (sequential stream scheduling). Streams are scheduled continuously in sequential order, with configurable number of packets per stream.</li> <li>• Burst. Packets in a stream are organized in bursts. Bursts from active streams form a burst group. The user specifies time from start of one burst group till start of next burst group.</li> </ul>

RECEIVE ENGINE	
Number of traceable Rx streams per port	2016 (wire-speed)
Automatic detection of test payload for received packets	Real-time reporting of statistics and latency, loss, payload integrity, sequence error, and disorder error checking
Jitter measurement	Jitter (Packet Delay Variation) measurements compliant to MEF10 standard with 1 ns accuracy . Jitter can be measured on up to 32 streams
Stream statistics 1)	<ul style="list-style-type: none"> <li>• RX Mbit/s, packets/s, packets, bytes.</li> <li>• Loss, payload integrity errors, sequence errors, disorder errors</li> <li>• Min latency, max latency, average latency</li> <li>• Min jitter, max jitter, average jitter</li> </ul>
Latency measurements accuracy	±16 ns
Latency measurement resolution	1 ns (Latency measurements can calibrate and remove latency from transceiver modules)
Number of filters	<ul style="list-style-type: none"> <li>• 6 x 64-bit user-definable match-term patterns with mask, and offset</li> <li>• 6 x frame length comparator terms (longer, shorter)</li> <li>• 6 x user-defined filters expressed from AND/OR'ing of the match and length terms</li> </ul>
Filter statistics	Per filter: RX Mbit/s, packets/s, packets, bytes
TX packet header support and RX auto decodes	Ethernet, Ethernet II, VLAN, ARP, IPv4, IPv6, UDP, TCP, LLC, SNAP, GTP, ICMP, RTP, RTCP, STP, MPLS, PBB, or fully specified by user
Packet scheduling modes	<ul style="list-style-type: none"> <li>• Normal (stream interleaved mode) – standard scheduling mode, precise rates, minor variation in packet inter-frame gap.</li> <li>• Strict Uniform – new scheduling mode, with 100% uniform packet inter-frame gap, minor deviation from configured rates.</li> <li>• Sequential packet scheduling (sequential stream scheduling). Streams are scheduled continuously in sequential order, with configurable number of packets per stream.</li> <li>• Burst. Packets in a stream are organized in bursts. Bursts from active streams form a burst group. The user specifies time from start of one burst group till start of next burst group.</li> </ul>
Rx Tap Settings	<ul style="list-style-type: none"> <li>• Freeze or Auto tune</li> </ul>

CAPTURE	
Capture criteria	All traffic, stream, FCS errors, filter match, or traffic without test payloads
Capture limit per packet	16 – 12288 bytes
Wire-speed capture buffer per port	64 kB
Low speed capture buffer per port (10Mbit/sec)	4096 packets (any size)

HW SPECIFICATIONS	
Max. Power	TBA W
Weight	2.32 lbs (1.05 kg)
Environmental	<ul style="list-style-type: none"> <li>Operating Temperature: 10 to 35° C</li> <li>Storage Temperature: -40 to 70° C</li> <li>Humidity: 8% to 90% non-condensing</li> </ul>
Regulatory	FCC (US),CE (Europe)
Connector insertions	<p>Xena uses high-quality 112Gbps-capable electrical connectors on Z800 Freya modules for optimal signal integrity and performance. However, all connectors experience wear when inserted, resulting in decreased signal integrity over time. The specification below is the minimum number of insertions where optimal signal integrity is guaranteed:</p> <ul style="list-style-type: none"> <li>Connectors, minimum number of guaranteed insertions: 500 cycles</li> </ul>
Notes	<ul style="list-style-type: none"> <li>This module is only supported by the B2400 and the XenaCompact chassis</li> <li>This module requires two slots in the B2400 chassis</li> </ul>

## Ordering Information

### Product Description

- Z800qc Freya QSFP in 1U Compact Chassis 5-speed 800Gbps (112/56G SerDes) dual-media test module
- Z800q Freya QSFP 800GE 5-speed 800Gbps 56G/112G PAM4 SerDes test module
- Z800oc Freya OSFP in 1U Compact Chassis 5-speed 800Gbps (112/56G SerDes) dual-media test module
- Z800o Freya OSFP 800GE 5-speed 800Gbps 56G/112G PAM4 SerDes test module

### Product Code

C-Freya-800G-4S-1P  
 Freya-800G-4S-1P  
 C-Freya-800G-4S-1P-OSFP  
 Freya-800G-4S-1P-OSFP



Local sales offices are located throughout the world. Visit our website to find the most convenient location.

1-800-5-LeCroy • [teledynelecroy.com](http://teledynelecroy.com)

