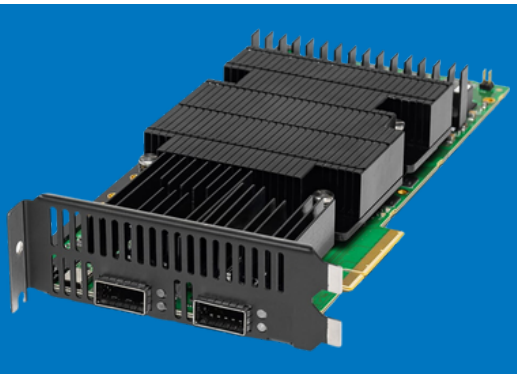
TELEDYNE LECROY
Everywhereyoulook™

Z800q Freya

5-speed 800Gbps (112/56G SerDes) dual-media test module



Key Features

- 5-speeds: 800GE, 400GE, 200GE, 100GE & 50GE
- Dual media: QSFP-DD800 & QSFP112
- Supports 112G SerDes (PAM4 112G) & 56G SerDes (PAM4)
- Test with optics and DAC's
- Auto-Negotiation & Link Training (AN/LT)
- Advanced Physical Layer testing
- Price/performance
- Ease of use

FIND OUT MORE HERE:

The Z800q Freya test module supports five different Ethernet network speeds - 800GE, 400GE, 200GE, 100GE and 50GE using 112G/56G SerDes (PAM4 112G/56G).

This flexibility is provided via two physical transceiver cages – one supporting QSFP-DD800 compatible transceivers, and the other supporting QSFP112 compatible transceivers.

Z800 Freya is a highly versatile solution designed for performance and functional testing of Ethernet network infrastructure and equipment including switches, routers and NICs.

Z800q Freya is unique on the market with its ability to test up to 800GE with 112G SERDES (PAM4 112G) meeting the highest demands for superior signal integrity and bit error rate performance.

Z800q Freya supports extensive L1 test features for advanced PCS and PMA layer testing including dynamic transceiver clock sweep, lane skewing and PRBS modes. Signals can be analyzed in advanced signal integrity view, which provides visual information on the quality of the signal.

The Z800q Freya test module supports Auto-Negotiation and Link Training (AN/LT) on 112G SerDes and 56G SerDes.

Z800q Freya modules can be installed in Xena B2400 chassis for multi-module setup, or delivered in the XenaCompact chassis, making it the most compact and lightweight 800G Ethernet test solution in the market.

With XenaManager users have access to an intuitive user-friendly multi-user management software where they can generate and analyze traffic. Xena OpenAutomation (XOA) enable customers to make the most of Xena testers with tailored tests as well as standardized test methodologies, to achieve accelerated release cycles, enhanced test reliability, and boosted customer satisfaction.

Ethernet Auto-Negotiation & Link Training Test Tools

Z800 Freya customers can purchase Z800 Freya-ANLT license for enabling AN/LT Utility on Z800q Freya and Z800o Freya OSFP modules. This license enables additional AN/LT tools for thorough testing of the endpoint behaviour during AN and LT process.

The AN/LT Utility provides insight, visibility, and configuration possibilities to the AN and LT process making it easy to analyze DUT behaviour during AN/LT, configure and optimize the relevant AN parameters and LT coefficients.

PORT LEVEL FEATURES	
Interface category	• **QSFP-DD800** 800G, 400G, 200G, 100G, 50G Ethernet • **QSFP112** 400G, 200G, 100G, 50G Ethernet
Total number of test ports (software configurable)	1x800G, 2x400G, 4x200G, 8x100G or 8x50G Ethernet
Interface options	QSFP-DD800 cage IEEE 112G SerDes: 1 x 800GE PAM4 802.3df (D2.0) / ETC* or 2 or 1 x 400GE PAM4 802.3ck or 4 or 2 x 200GE PAM4 802.3ck or 8 or 4 x 100GE PAM4 802.3ck 56G Serdes: 1 x 400GE PAM4 802.3bs or 802.3cd 2 x 200GE PAM4 802.3cd or 4 x 100GE PAM4 802.3cd or 8 x 50GE PAM4 802.3cd QSFP112 cage 112G SerDes: 1 x 400GE PAM4 802.3ck or 2 x 200GE PAM4 802.3ck or 4 x 100GE. PAM4 802.3ck 56G Serdes: 1 x 400GE PAM4 802.3bs or 802.3cd 2 x 200GE PAM4 802.3cd or 4 x 100GE PAM4 802.3cd or 8 x 50GE PAM4 802.3cd Both cages must run with the same interface configuration (e.g. 4 x 100G) and same SerDes speed (e.g 112G) *ETC = Ethernet Technology Consortium
Auto Negotiation and Link Training	Auto-negotiation: IEEE 802.3 Clause 73 and ETH. 400G/800G specifications Link training: IEEE 802.3 Clause 136 and 161
Forward Error Correction (FEC)	RS-FEC (Reed-Solomon) (544,514,t=15), IEEE802.3 Clause 119 RS-FEC (Reed-Solomon) (544,514,t=15), IEEE802.3 Clause 134
Number of transceiver module cages	1 x QSFP-DD800 and 1 x QSFP112
Port statistics	Link state, FCS errors, pauseframes, ARP/PING, error injections, training packet All traffic: RX and TX Mbit/s, packets/s, packets, bytes Traffic w/o test payload: RX and TX Mbit/s, packets/s, packets, bytes
Adjustable Inter FrameGap (IFG)	Configurable from 16 to 56 bytes, defaultis 20B (12BIFG + 8B preamble)
Transmit line rate adjustment	Ability to adjust the effective line rate by forcing idle gaps equivalent to -1000 ppm (increments of 10 ppm)
Transmit line clock adjustment	From -400 to 400 ppm in steps of 1 ppm (shared across all ports)
PPM Sweep	Configurable linear or step sweep +/- 400 ppm

ARP/PING	Supported (configurable IP and MAC address per port)
Field upgradeable	System is fully field upgradeable to product releases (FPGA images and software)
Tx disable	Enable/disable of optical laser or copperlink
Field upgradeable	System is fully field upgradeable to product releases (FPGA images and software)
IGMPv2 multicast join/leave	IGMPv2 continuous multicast join, with configurable repeat interval
Histogram statistics	Two real-time histograms per port. Each histogram can measure one of RX/TX packet length, IFG, or Latency distribution for all traffic, a specific stream, or a filter
Loopback modes	• L1RX2TX – RX-to-TX, transmit byte-by-byte copy of the incoming packet • TXON2RX – TX-to-RX, packet is also transmitted from the port • TXOFF2RX – TX-to-RX, port's transmitter is idle
Oscillator characteristics	• Initial Accuracy is 3 ppm • Frequency driftover 1st year:+/- 3 ppm (over 15 years: +/- 15 ppm) • Temperature Stability: +/- 20 ppm (Total Stability is +/- 35 ppm)

PCS/PMA LAYERS TESTING	
Payload Test pattern	PRBS-13 & PRBS-31
Alarms	PRBS pattern loss, link sync loss
Error analysis	Bit-errors: seconds, count, rate
PCS virtual lane configuration	User-defined skew insertion per Tx virtual lane, and user-defined virtual lane-to-SerDes mapping for testing of the Rx PCS virtual lane reorder function
PCS virtual lane statistics	Relative virtual lane skew measurements (up to 2048 bits) Corrected Bit error, Pre-FEC BER
FEC Total statistics	Total corrected FEC symbols,Total uncorrected FEC symbols,Estimated Pre-FEC BER Estimated Post-FEC BER, Pre-FEC Error Distribution Graph
Link Flap	Single shot or repeatable link-down events with ms precision
Error Injection (PMA Layer)	Repeatable error injectperiods at PMA layer with ms precision

PHY/TRANSCEIVER ETHERNET TESTING	
Programmable Pattern Generator	• Supported in ANLT mode • Single stream Ethernet frames with FCS • Traffic load: up to 100% • Configurable Frame Size distribution and content • Transmit and Receive Statistics

ADVANCED PHY FEATURES	
Equalization Controls	Tx Transmit Equalization Controls • Pre-emphasis • Attenuation • Post-emphasis Rx Receive Equalization Controls • Continuous Time Linear Equalizer
Signal Integrity Analysis	Advanced signal integrity view

TRANSMIT ENGINES	
Number of transmit streams per port	256 (wire-speed) Each stream can generate millions of traffic flows using field modifier
Test payload insertion per stream	Wire-speed packet generation with timestamps, sequence numbers, and data integrity signature optionally inserted into each packet.
Stream statistics	TX Mbit/s, packets/s, packets, bytes, FCS error
Bandwidth profiles	Burst size and density can be specified. Uniform and bursty bandwidth profile streams can be interleaved
Field modifiers	24-bit header field modifiers with incremental, decremental, or random mode. Each modifier has configurable bit-mask, repetition, min, max, and step parameters. Eight 24-bit modifiers can be configured per stream
Packet length controls	Fixed, random, butterfly, and incrementing packet length distributions from 56 to 16k bytes
Packet payloads (basic)	Repeated userspecified 1 to 18B pattern, an 8-bit incrementing pattern
Error generation	Undersize length (56 bytes min) and oversize length (12288 bytes max.) packet lengths, injection of sequence, misorder, payload integrity, and FCS errors

TX packet header support and RX auto decodes	Ethernet, Ethernet II, VLAN, ARP, IPv4, IPv6, UDP, TCP, LLC, SNAP, GTP, ICMP, RTP, RTCP, STP, MPLS, PBB, or fully specified by user
Packet scheduling modes	• Normal (stream interleaved mode) – standard scheduling mode, precise rates, minor variation in packet inter-frame gap. • Strict Uniform – new scheduling mode, with 100% uniform packet inter-frame gap, minor deviation from configured rates. • Sequential packet scheduling (sequential stream scheduling). Streams are scheduled continuously in sequential order, with configurable number of packets per stream. • Burst. Packets in a stream are organized in bursts. Bursts from active streams form a burst group. The user specifies time from start of one burst group till start of next burst group.

RECEIVE ENGINE	
Number of traceable Rx streams per port	2016 (wire-speed)
Automatic detection of test payload for received packets	Real-time reporting of statistics and latency, loss, payload integrity, sequence error, and misorder error checking
Jitter measurement	Jitter (Packet Delay Variation) measurements compliant to MEF10 standard with 1 ns accuracy . Jitter can be measured on up to 32 streams
Stream statistics 1)	• RX Mbit/s, packets/s, packets, bytes. • Loss, payload integrity errors, sequence errors, misorder errors • Min latency, max latency, average latency • Min jitter, max jitter, average jitter
Latency measurements accuracy	±16 ns
Latency measurement resolution	1 ns (Latency measurements can calibrate and remove latency from transceiver modules)
Number of filters	• 6 x 64-bit user-definable match-term patterns with mask, and offset • 6 x frame length comparator terms (longer, shorter) • 6 x user-defined filters expressed from AND/OR'ing of the match and length terms
Filter statistics	Per filter: RX Mbit/s, packets/s, packets, bytes

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CAPTURE	
Capture criteria	All traffic, stream, FCS errors, filter match, or traffic without test payloads
Capture limit per packet	16 – 12288 bytes
Wire-speed capture buffer per port	64 kB
Low speed capture buffer per port (10Mbit/sec)	4096 packets (any size)

HW SPECIFICATIONS	
Max. Power	TBA W
Weight	2.32 lbs (1.05 kg)
Environmental	• Operating Temperature: 10 to 35º C • Storage Temperature: -40 to 70º C • Humidity: 8% to 90% non-condensing
Regulatory	FCC (US),CE (Europe)
Connector insertions	Xena uses high-quality 112Gbps-capable electrical connectors on Freya modules for optimal signal integrity and performance. However, all connectors experience wear when inserted, resulting in decreased signal integrity over time. The specification below is the minimum number of insertions where optimal signal integrity is guaranteed: • Connector for QSFPDD : Minimum number of guaranteed insertions: 500 cycles • Connector for QSFP112 : Minimum number of guaranteed insertions: 500 cycles
Notes	• This module is only supported by the B2400 and the ValkyrieCompact chassis • This module requires two slots in the B2400 chassis

Ordering Information

Product Description	Product Code
• Z800qc Freya QSFP in 1U Compact Chassis 5-speed 800Gbps (112/56G SerDes) dual-media test module	C-Freya-800G-4S-1P
• Z800q Freya 800GE 112G PAM4 SerDes test module QSFP-DD800	Freya-800G-4S-1P