Z800qac Freya

Ethernet Auto-Negotiation & Link Training Test Appliance

Key Features

- Dedicated and optimized AN/LT tester

- Compact 1U 19" "desktop" format

- 5-speeds: 800GE, 400GE, 200GE, 100GE & 50G

- QSFP-DD800 & QSFP112 cage

- Supports 112G SerDes (PAM4) & 56G SerDes (PAM4)

- Auto-Negotiation & Link Training (AN/LT)

- Test DACs, ACCs and AN/LT Endpoints

- Comprehensive PCS & PMA layer test capabilities

- Ease of use

- Price/ Performance

- Advanced architecture

Find out more here:

The Z800qac Freya ANLT Test Appliance QSFP-DD is designed specifically for Ethernet AN/LT testing at 56G/112G PAM4 SerDes speeds.

Ideally Auto-Negotiation & Link Training are initiated automatically, and the two devices run through the different states in the protocols to negotiate speed and tune to optimal settings. However not all endpoints behave the same and interpretations and implementations of the standards varies. Also, the quality of the AN/LT training results are not always consistent which can lead to erratic link stability.

The Z800qac Freya ANLT Test Appliance allows thorough testing of the endpoint behaviour. It provides insight, visibility, and configuration possibilities to the AN and LT process making it easy to analyze DUT behaviour during AN/LT, and configure and optimize the relevant AN parameters and LT coefficients.

Leveraging Xena's award-winning Z800q Freya test modules, the Z800qac Freya is a small 1U "desktop" tester that is easy to transport from site to site in a 19" flight case. In addition to this QSFP-DD version, there is also a OSFP version (Z800oac Freya)

The advanced AN/LT test capabilities can also be enabled on "standard" Freya modules by purchasing a dedicated AN/LT Test Appliance license "Z800 Freya-ANLT".

Layer 1 Test Tools

The Z800 FreyaCompact ANLT Test Appliance includes XenaManager, Xena's user-friendly management software which supports the same L1 features as the Freya test modules incl.: PRBS, single stream TGA for PHY/PCS testing, Advanced PMA and PCS/FEC Error Injection, lane skewing & swapping, and ppm sweeping.

AN/LT Testing

Also included is the Xena OpenAutomation (XOA) AN/LT Test Utility and the AN/LT Protocol Test Suite for performance and conformance testing.

The Xena OpenAutomation (XOA) AN/LT Test Utility is a command line tool for Interactive AN/LT Protocol Testing with single stepping of the LT protocol towards the DUT while providing statistics and logging.

The Xena OpenAutomation (XOA) AN/LT Test Suite is designed for performance and compliance testing. It can be orchestrated from third party analyzers or automation systems through its REST API or run as a stand-alone application together with the XOA AN/LT Test Suite Application.

PORT LEVEL FEATURES	
Interface category	QSFP-DD800 - 800G, 400G, 200G, 100G, 50G Ethernet QSFP112 - 400G, 200G, 100G, 50G Ethernet
Total number of test ports (software configurable)	1x800G, 2x400G, 4x200G, 8x100G and 8x50G Ethernet
Interface options	**QSFP-DD800 cage** 112G SerDes: IEEE • 1 x 800GE PAM4 802.3df (D2.0) / ETC* or • 2 or 1 x 400GE PAM4 802.3ck or • 4 or 2 x 200GE PAM4 802.3ck or • 8 or 4 x 100GE PAM4 802.3ck 56G SerDes: • 1 x 400GE PAM4 802.3bs or • 2 x 200GE PAM4 802.3cd or • 4 x 100GE PAM4 802.3cd or • 8 x 50GE PAM4 802.3cd **QSFP112 cage** 112G SerDes: • 1 x 400GE PAM4 802.3ck or • 2 x 200GE PAM4 802.3ck or • 4 x 100GE PAM4 802.3ck 56G SerDes: • 1 x 400GE PAM4 802.3ck or • 2 x 200GE PAM4 802.3ck or • 4 x 100GE PAM4 802.3ck or • 8 x 50GE PAM4 802.3ck Both cages must run with the same interface configuration (e.g. 4 x 100G) & same SerDes speed (e.g 112G) Power capacity using single cage: QSFP-DD800: 25W or QSFP112: 15W Power capacity using both cages: QSFP-DD800: 15W + QSFP112: 15W *ETC = Ethernet Technology Consortium
Forward Error Correction (FEC)	RS-FEC (Reed Solomon) (544,514,t=15), IEEE 802.3 Clause 119, Clause 134
Port statistics	Link state, FCS errors, error injections, RX and TX Mbit/s, packets/s, packets, bytes
Adjustable Inter Frame Gap (IFG)	Configurable from 16 to 56 bytes, default is 20B (12B IFG + 8B preamble)
Transmit line rate adjustment	Ability to adjust the effective line rate by forcing idle gaps equivalent to -1000 ppm (increments of 10 ppm)
Transmit line clock adjustment	From -400 to 400 ppm in steps of 1 ppm
PPM Sweep	Configurable linear or step sweep +/- 400 ppm
Field upgradeable	System is fully field upgradeable to product releases (FPGA images and software)
Loopback modes	• TXON2RX – TX-to-RX, packet is also transmitted from the port • TXOFF2RX – TX-to-RX, port's transmitter is idle • Layer 1 RX2TX – PCS-layer loopback (TX not frequency locked to RX)

PCS/PMA LAYERS TESTING	
Payload Test pattern	PRBS-31
Alarms	PRBS pattern loss, link sync loss
Error analysis	Bit-errors: seconds, count, rate
PCS virtual lane configuration	User-defined skew insertion per Tx virtual lane, and user-defined virtual lane to SerDes mapping for testing of the Rx PCS virtual lane re-order function
PCS virtual lane statistics	Virtual lane skew measurements (up to 2048 bits) Corrected Bit error, PreFEC
FEC Total statistics	Total corrected FEC symbols, Total uncorrected FEC symbols, Estimated Pre-FEC BER, Estimated Post-FEC, Pre-FEC Error Distribution Graph
Link Flap	Single short or repeatable link down events with ms precision
Error Injection (PMA Layer)	Repeatable (burst) error inject periods at PMA layer with ms precision and configurable BER
Error Injection (PCS/FEC Layer)	- Deterministic injection of symbol errors in FEC codewords - Generation of sequences of FEC codewords with deterministic error distribution

AN/LT Testing	
Auto Negotiation and Link Training	Auto-negotiation: IEEE 802.3 Clause 73 and Ethernet Technology Consortium 400G/800G specification Link training: IEEE 802.3 Clause 136 or 161
AN/LT protocol testing	Command line tool for Interactive AN/LT Protocol Testing with single step of the LT protocol towards DUT with Xena OpenAutomation (XOA) AN/LT Test Utility
Performance and compliance testing of AN/LT	Can be performed with Xena OpenAutomation (XOA) AN/LT Test Suite, or orchestrated from 3rd party analyzers or automation systems

PHY/TRANSCEIVER ETHERNET TESTING	
Traffic generation	Ethernet frames with FCS Traffic load: up to 100% Configurable Frame Size distribution and content

ADVANCED PHY FEATURES	
Equalization Controls	Tx Transmit Equalization Controls • Pre-emphasis • Attenuation • Post-emphasis Auto-Tune or manual control of Rx equalizer (FFE/DFE/CTLE)
Signal Integrity Analysis	Advanced signal integrity view
Jitter measurement	• Jitter (Packet Delay Variation) measurements compliant to MEF10 standard • with 8 ns accuracy • Jitter can be measured on up to 32 streams

TRANSMIT ENGINES	
Number of transmit streams per port	1 (wire-speed)
Test payload insertion per stream	Wire-speed packet generation
Stream statistics	TX Mbit/s, packets/s, packets, bytes, FCS error
Bandwidth profiles	Burst size and density can be specified. Uniform and bursty bandwidth profile streams can be interleaved
Packet length controls	Fixed, random, butterfly, and incrementing packet length distributions from 56 to 12288 bytes
Packet payloads (basic)	Repeated user specified 1 to 18B pattern, an 8-bit incrementing pattern
Packet scheduling modes	Normal (stream interleaved mode) – standard scheduling mode, precise rates, minor variation in packet inter-frame gap

RECEIVE ENGINE	
Number of traceable Rx streams per port	1 (wire-speed)
Stream statistics	RX Mbit/s, packets/s, packets, bytes

HW SPECIFICATIONS	
Oscillator characteristics	Initial Accuracy is 3 ppm • Frequency drift over 1st year: +/- 3 ppm (over 15 years: +/- 15 ppm) • Temperature Stability: +/- 20 ppm (Total Stability is +/- 35 ppm)
AC Voltage	100-240V
Frequency	50-60Hz
Max. Current	2A with 120V supply, and 1A with 240V supply
Max. Power	220W
Weight	16.5 lbs (7.5 kg)
Environmental	Operating Temperature: 10 to 35º C Storage Temperature: -40 to 70º Humidity: 8% to 90% non-condensing
Dimensions	W: 19" (48.26 cm) H: 1.75" (4.45 cm) D: 15" (37 cm)
Max. Noise	67 dBA
Regulatory	FCC (US), CE (Europe)
Notes	Xena uses high-quality 112Gbps-capable electrical connectors on Freya modules for optimal signal integrity and performance. However, all connectors experience wear when inserted, resulting in decreased signal integrity over time. The specification below is the minimum number of insertions where optimal signal integrity is guaranteed: • QSFP-DD Connector: Min. number of guaranteed insertions: 500 cycles • QSFP112 Connector: Min. number of guaranteed insertions: 500 cycles

Ordering Information

Product Description
Z800qac Freya-QSFP-DD Ethernet Auto-Negotiation & Link Training Test Appliance

Product Code
C-Freya-800G-ANLT-QSFP-DD